UNITED STATES PATENT AND TRADEMARK OFFICE

I, John Barton COATES BSc, CEng, MIEE,

translator to RWS Group plc, of Europa House, Marsham Way, Gerrards Cross, Buckinghamshire, England declare;

1. That I am a citizen of the United Kingdom of Great Britain and Northern Ireland.

2. That I am well acquainted with the German and English languages.

3. That the attached is, to the best of my knowledge and belief, a true translation into the English language of the specification in German filed with the application for a patent in the U.S.A. on March 26, 2003

under the number 60/457,811

4. That I believe that all statements made herein of my own knowledge are true and that all statements made on information and belief are true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the patent application in the United States of America or any patent issuing thereon.

For and on behalf of RWS Group plc

The 22nd day of August 2003

ANNEX A:

Programmable amplifier with simple signal equalization
Inventor: Peter Gregorius, COM ON CE

1. What technical problem is intended to be solved by your invention?

Equalization of data pulses which are severely distorted by a transmission line/channel. Band limiting of the transmission channel results in the signal at the receiver being subject to distortion caused by intersymbol interference.

Particular requirements:

- Severe distortion caused by band limiting of the transmission channel.
- Reflections (echo) caused by incorrect matching to the line impedance, both at the transmitting end and at the receiving end.
- Resonances in the transmission characteristic of the channel
- Small eye opening and distorted pulse

2. How has this problem been solved until now? What disadvantages were associated with this?

In contrast to lower-frequency applications for data transmission (for example 2Mbit/s band), complex equalization of the data stream upstream of a data recovery unit (for example clock and data recovery, CDR) is not possible. Methods which are based on oversampling by means of analog/digital converters and digital equalization (for example Viterbi decoders, Decision Feedback Eq. etc.) can generally not be used for very high data rates, for technological reasons (maximum bandwidth of semiconductor technology).

At present, the preamplifiers for data transmission applications via PCB or back-plane connections are generally simple limiting amplifiers. The only aim here is to maximize the eye opening, that is to say the amplitude of the signal, in order that the downstream data recovery unit has as much signal energy as possible with the best possible signal-to-noise ratio (SNR) for evaluation at the decision time.

This apparent improvement in the SNR by signal limiting can be argued to be valid only for as long as the input signal to be amplified is not subject to major edge and/or amplitude noise. However, in reality, the signal is generally noisy. The consequence of simple limiting is AM-to-PM conversion, that is to say conversion of the amplitude error to increased edge noise. Error-free recovery of the signal thus becomes considerably more difficult for the downstream data recovery unit, in this case generally a clock and data recovery circuit or timing recovery circuit. A worse bit error rate can generally be expected. The maximum possible range and the maximum permissible attenuation of the channel are in consequence restricted. This is contrary to the requirement for high data rates over relatively highly band-limited transmission paths.

One possible solution is to use complex adaptation methods. There are two major options for this - a linear feed forward equalizer FFE or an equalizer with feedback, such as decision feedback. Other equalizers, which are based on statistical methods, can be used only to a limited extent at these data rates owing to the lack of additional information in the data stream, for example a preamble. This is a purely stochastic data stream. Implementation of the stated methods - for example decision feedback - generally requires considerable complexity to implement it.

3. How does your invention solve this problem, and what advantages does this solution offer?

The invention combines discrete-time methods with continuous-time methods for equalization of the data signal, in particular for high-speed serial data transmission, in which quantization of the signal is impossible or is too complex. This method offers a capability for simple signal equalization without feedback. In most (multichannel) high-speed links, the necessary phases for the equalizer are required in any case for the subsequent timing recovery. Only a small amount of additional circuit complexity is thus required. Furthermore, this unit can be designed such that it can be adjusted as required - until the circuit function is reduced to that of a normal limiting amplifier. In addition, the gain levels/coefficients can be programmed.

Basic operation: Figure 1 (a) shows the timing of a signal profile. A trapezoidal signal is applied to the transmission path at the transmitter. The band limiting in the transmission path leads to the impulse response as shown in the center of Figure 1 (a). The trailing edge of the impulse response leads, with a high data density, to superimpositions of the individual impulse responses - the signal is distorted. The desired impulse response at the receiver is illustrated at the bottom of Figure 1 (a). In order to obtain this impulse response, it is necessary to subtract the appropriate time components from the actual impulse response.

When using continuous-time methods in this case, the inverse of the transfer function of the channel is formed. Mathematically, this can be described in the Laplace plane as follows:

$$H_{equ}(s) = \frac{1}{H_{channel}(s)} = \frac{A \cdot \prod_{k=1}^{n}(1 + s/\omega_{zk})}{\prod_{k=1}^{m}(1 + s/\omega_{pk})} \qquad \text{(Equation 3.1)}$$

The following function is obtained for the outline circuit diagram shown in Figure 1 (b):

$$H_{equ}(s) = \frac{U_{out}}{U_{in}}(s) = A_2 - A_1 \frac{1}{(1 + s/\omega_{1k})} \qquad \text{(Equation 3.2)}$$

$$H_{equ}(s) = \frac{U_{out}}{U_{in}}(s) = A_2 - A_1 \frac{1}{\prod_{k=1}^{m}(1 + s/\omega_{pk})} \qquad \text{(Equation 3.3)}$$

Equation 3.3 illustrates the general representation of the implementation variant of the transfer function for approximation of the channel transfer function. This implementation has the advantage that pole positions are required only for approximation - this is particularly advantageous for stability criteria.

In a discrete-time representation, the transfer function according to equation 3.3 can be represented as follows:

$$H_{equ}(z) = \frac{U_{out}}{U_{in}}(z) = A_2 - A_1 \frac{1}{1 + \prod_{k=1}^{n}(b_{bk} \cdot z^{-k\tau})} = A_2 - A_1 \frac{1}{1 + b_{b1} \cdot z^{1\tau} + b_{b2} \cdot z^{-2\tau} + ... + b_{bn} \cdot z^{-n\tau}}$$

(Equation 3.4)

Equation 3.4 provides the basic formal relationship to implement the invention.

4. What is the essence of your invention?

A combination of discrete-time and continuous-time methods for equalization by means of current-mode

circuit technology for high-speed serial data transmission. The formal relationship, as shown in equation 3.3 or 3.4, for approximation of the channel can be implemented by the invention both on a continuous-time basis and on a discrete-time basis.

5. Exemplary embodiment and/or implementation

Variant 1: This variant comprises what is referred to as a delay locked loop (DLL) and the arrangement according to the invention. The DLL is formed from the elements 10 to 17. The arrangement according to the invention is represented by the elements 1 to 9.

Operation of the DLL: The DLL is formed from an input amplifier 10, the delay elements 11 to 14, the amplifier 17, the phase detector 15 and the low-pass filter LPF 16. The operation of the DLL can be described easily. The clock CLK_{in} at the input is passed to the phase detector 15 by means of the delay elements 11 to 14. In parallel with the delayed signal at the phase detector input, the input signal is passed without being delayed to the phase detector. The phase detector compares the phase of the two input signals and passes a manipulated variable, which is proportional to the phase difference, to the loop filter. The loop filter uses a desired cut-off frequency to filter the disturbance variables out of the manipulated variable, and feeds the manipulated variable in at the output of the filter at the control input of the delay elements DT1 to DTn. Depending on the version, the DLL regulates the two signals at the input of the phase detector to a phase difference of 180° or 360°. The signal phases N/PCLK_1 to N/PCLK_n have an equidistant phase separation.

Operation of the arrangement for equalization: The equalizer comprises the input amplifier 1, the delay elements 2 to 5, the multiplexer 6, the summation point

8, the amplifier 9 and the (optional) downstream isolation amplifier (or limiter) 7. The arrangement provides a transfer function as in equation 3.4. The delay elements 2 to 5 comprise the delay unit DT1..n and the amplifier A11..1n. The delay element DT1..n is preferably identical in design to the delay elements within the DLL. In addition, the amplifier unit A11..1n is programmable. The delay elements DT1..n in this case form the delays nxt from equation 3.4. The amplifiers form the coefficients $b_{b1..n}$. The overall delay is obtained from the sum of the individual delays.

The delay within a delay element is implemented in such a way that the delay element disconnects the input signal with the rising edge of CLK_1..n of the differential clock signal P/NCLK_1..n toward the amplifier. The signal from the delay element is passed to the next delay element, while the weighted signals from the amplifiers A11 to A1n are passed to the multiplexer.

Depending on the desired equalization depth, the number of elements can be varied, or, in the application, can be matched by suitable coefficients (gain).

At the summation point, the weighted signals and the undelayed signal are joined together. The signal, which has now been equalized, can additionally be amplified (or limited) by a further amplifier stage.

The advantage of this implementation is the capability to implement it with simple analog circuitry (for example current mode), quasi-digital operation with a wide bandwidth at the same time, and, possibly, differential signal routing - that is to say the advantages of simple digital signal processing can be combined with the advantages of a broadband, interference-resistant, analog implementation for signal equalization.

Variant 2: Variant 2 differs from variant 1 by the continuous-time signal processing. This circuit arrangement passes the control signal at the output of the loop filter of the DLL both to the delay elements of the DLL and to the equalization. This variant results in a transfer function as in equation 3.3.

Variant 3: In contrast to variants 1 and 2, each delay element within the cell contains a summation point and the additional amplifier An2. The advantage is the complex structure, which can be implemented in a particularly advantageous manner using analog circuitry. An example of this is shown in Figure 6. Depending on the programming, the equalizer can operate with 1, 2 or any n desired stages. For this purpose, in a corresponding manner, the delayed and weighted signal from the previous stage n is passed to the summation point of the next stage n+1. The control is in this case provided from the subsequent stage by the signal CS(n+1). The summation of the previous stage n is no longer taken into account. The equalized signal from the stage n+1 can now be selected via the multiplexer. The advantage is the simple circuitry.

The left-hand half of the illustration in Figure 6 shows a transistor circuit in which a cell as shown in Figure 4, variant 3 is illustrated. The transistor pairs MN1 and MN6, MN2 and MN5 as well as MN3 and MN4 form a differential amplifier. The summation point is formed as the current sum in the resistor RL. The difference pair MN3 and MN4 is in this case representative of the amplifier A2n. The transistors MN1, MN6, MN2 and MN5 form the amplifier A1n. The transistors MN8 and MN9 switch the foot I02, which can be set as a function of Bn[y:0]. If the signal is intended to be passed to the next stage n+1, then PCS becomes positive and NCS negative. The complete current I02 is now passed to the difference pairs MN2/MN5. The

gradient of the transistors MN1, MN2, MN5 and MN6 is ideally the same.

The transistors MN3 and MN4 are driven from the amplifier A0 as shown in Figure 4, variant 3. The delay elements DTn may be in any desired form. However, it is once again advantageous in this case for both elements to be an arrangement based on difference stages.

The right-hand half of the illustration in Figure 6 shows a cascaded arrangement. The outputs VN1n and VP1n are in this case connected to the summation point of the stage n+1. The signals VN2n, VP2n, VN2(n+1) and VP2(n+1) are passed to the multiplexer, as shown in Figure 4, variant 3. The signals VN3n and VP3n are connected only to the next difference pair (MN3 & MN4) in this stage.

The advantage of this arrangement is the completely symmetrical structure, which allows differential signal processing. The layout can be optimally matched to the signal flow, and signal line crossings can be avoided to the maximum extent. This is particularly advantageous for radio-frequency applications.

An implementation as shown in Figure 2, variant 1 can be used to control the delay cell.

Variant 4: By contrast to the variant 3, the delay element is in this case provided as shown in Figure 3, variant 2.

Variant 5: In variant 5, all the elements are controlled by means of a digital word from the central control unit.

6. What steps are required for verification of your invention in a competitor product?

Product analysis and measurements.

8. Literature

a) [1] IEEE, JSSC, April 1997
NRZ Timing Recovery Technique for Band-Limited Channels
Bang-Sup Song

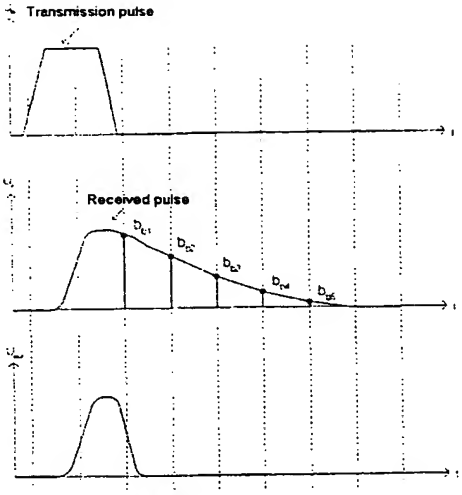

Figure 1a

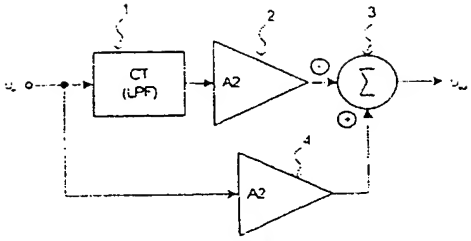

Figure 1b

Figure 1: Impulse response of a band-limited channel (a) and a continuous-time method for equalization (b)

Variant 1

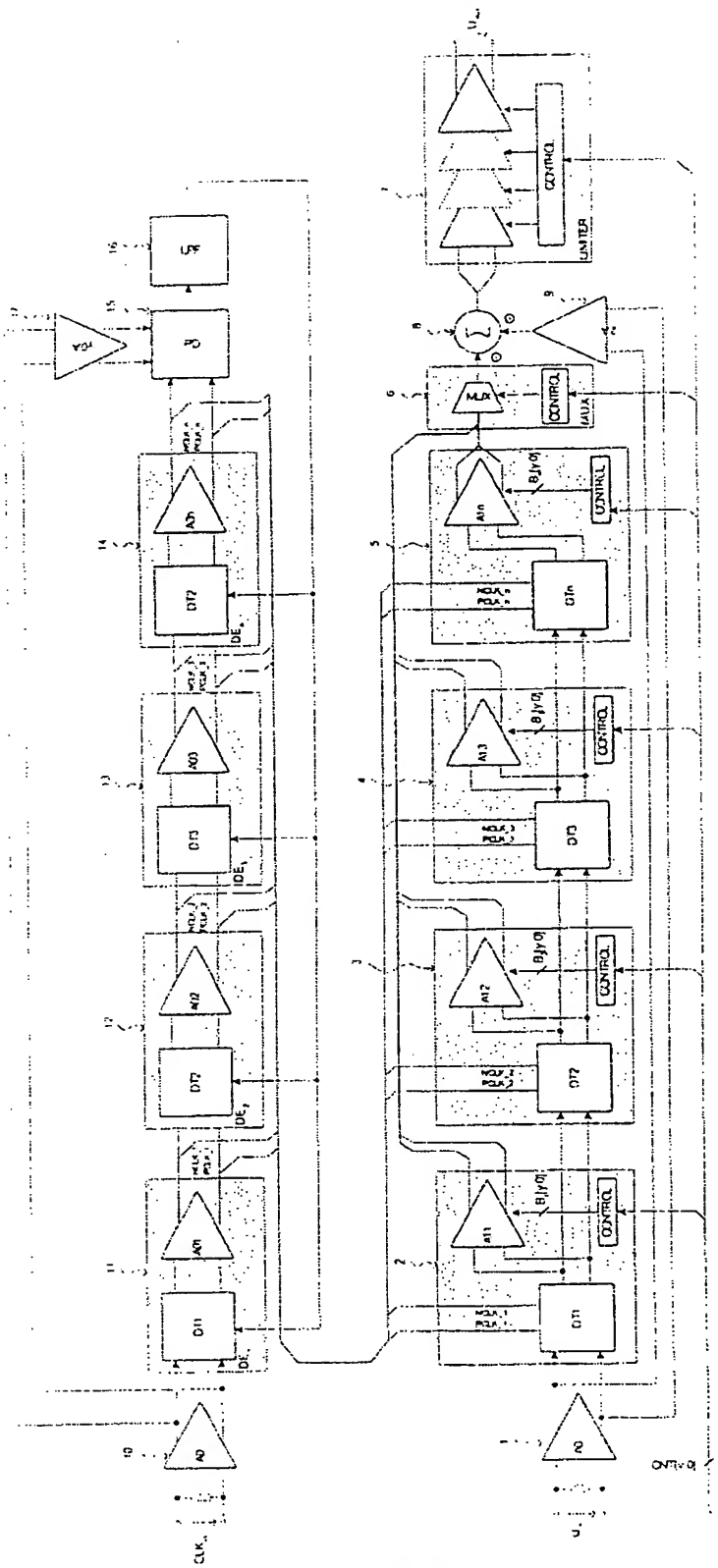

Figure 2: Variant 1 for implementation

Variant 2

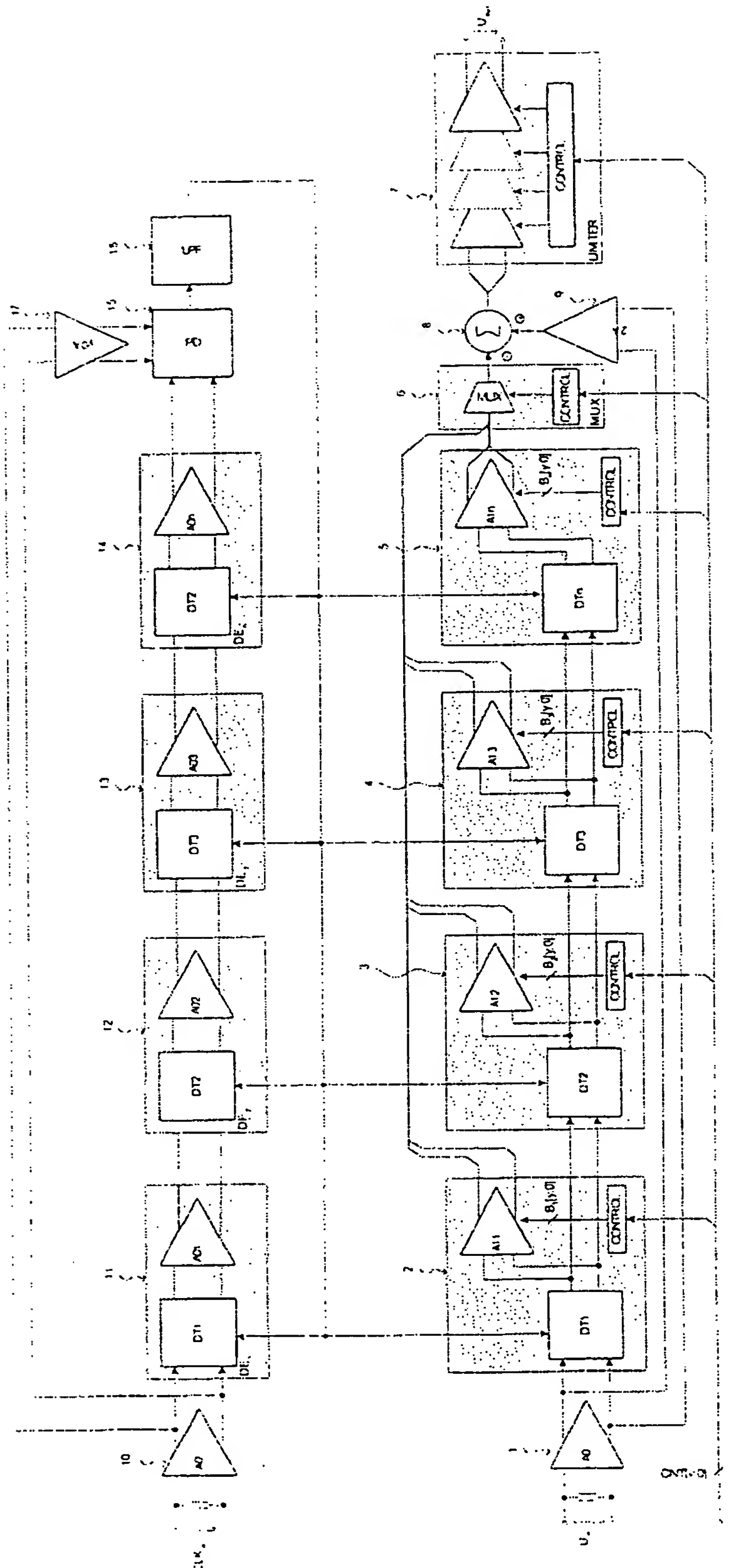

Figure 3: Variant 2 for implementation

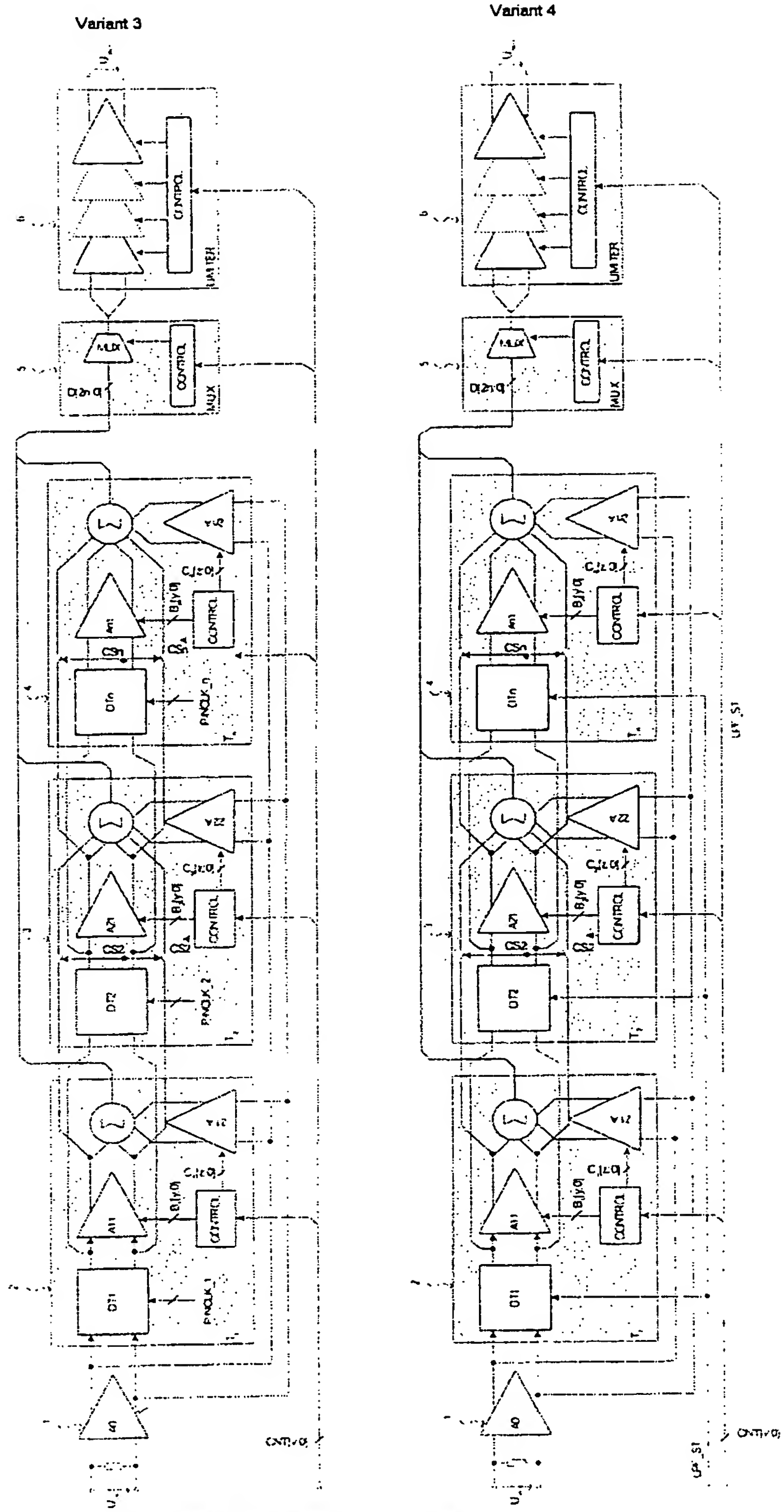

Figure 4: Variant 3 and variant 4 for implementation

Variant 5

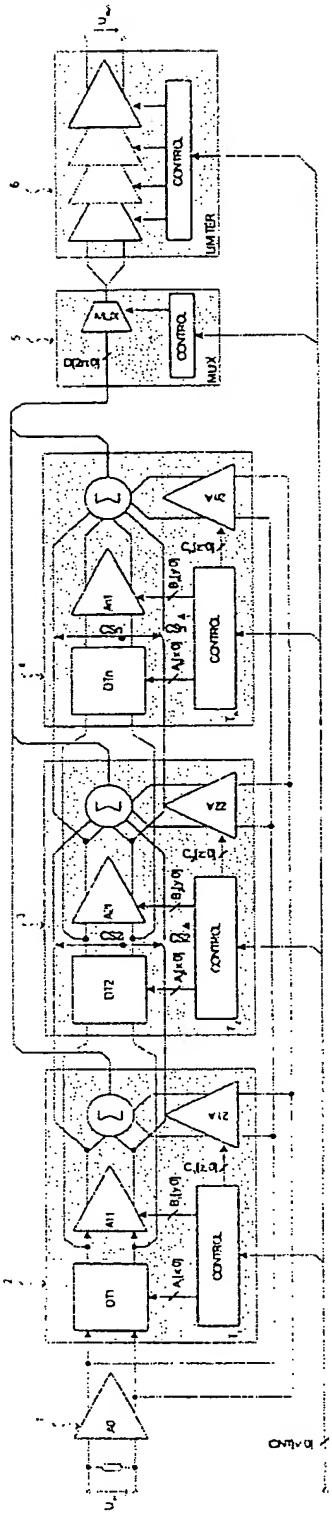

Figure 5: Variant 5 for implementation

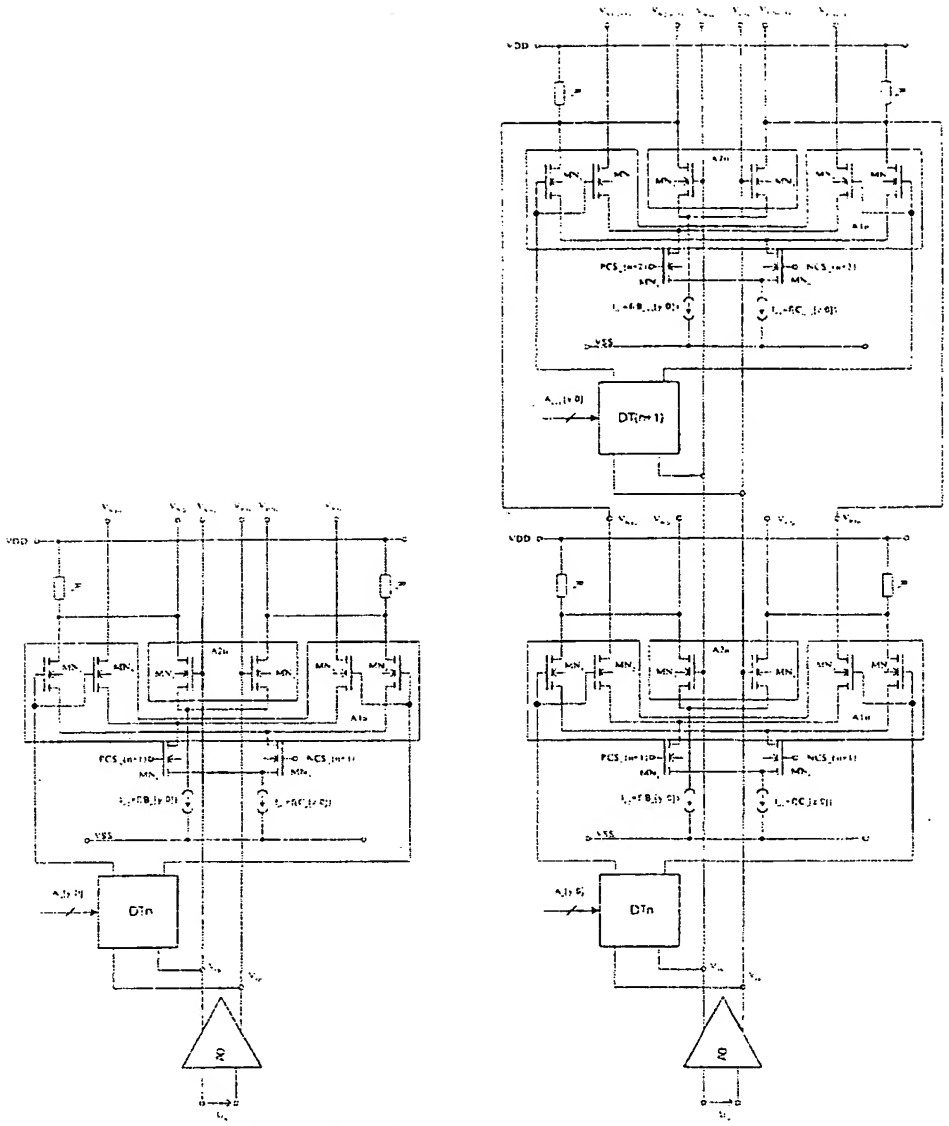

Figure 6: Possible implementation of a delay unit with an amplifier according to variants 3, 4 and 5.